

09/597974

Figure 1

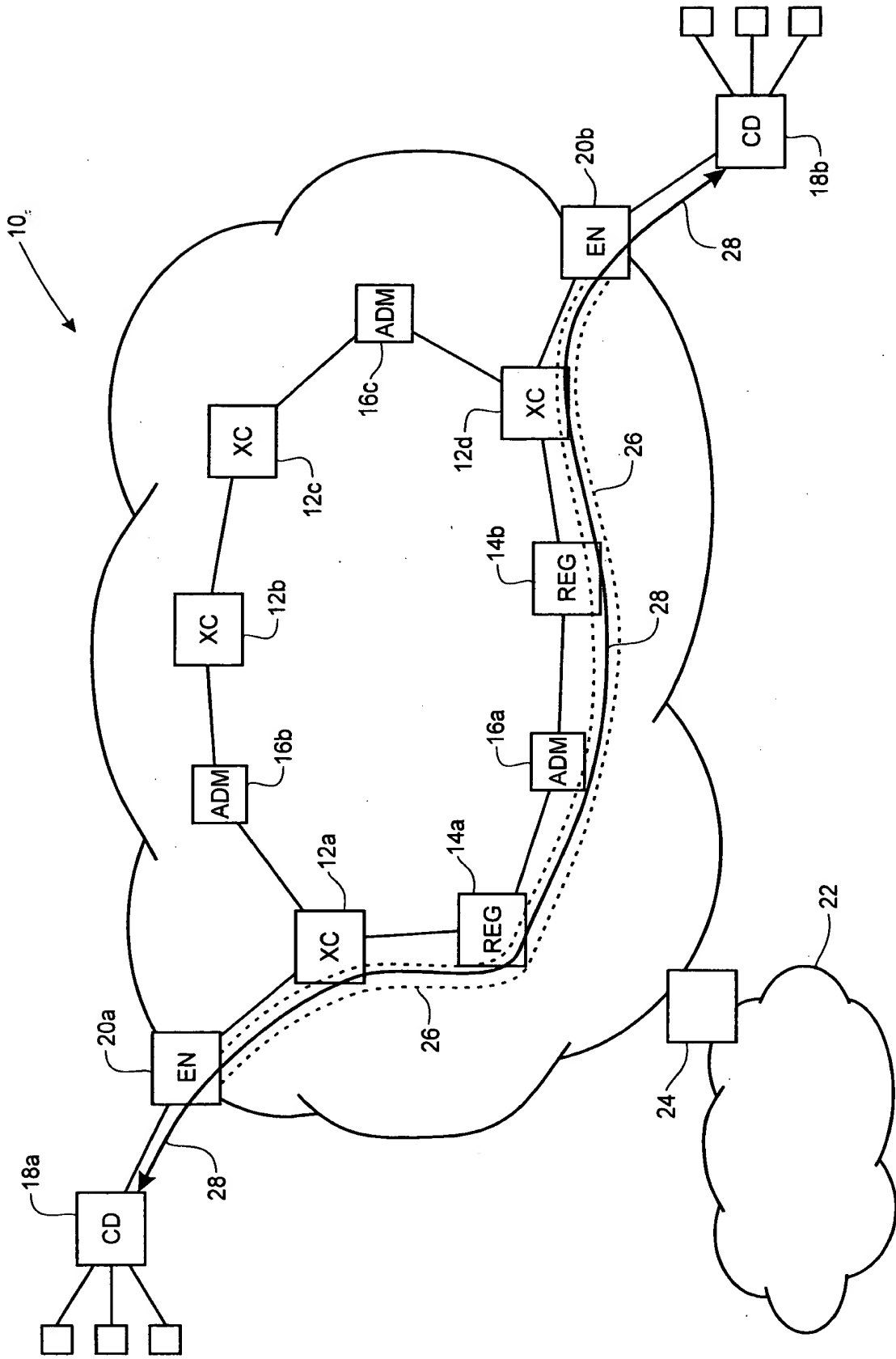


Figure 2

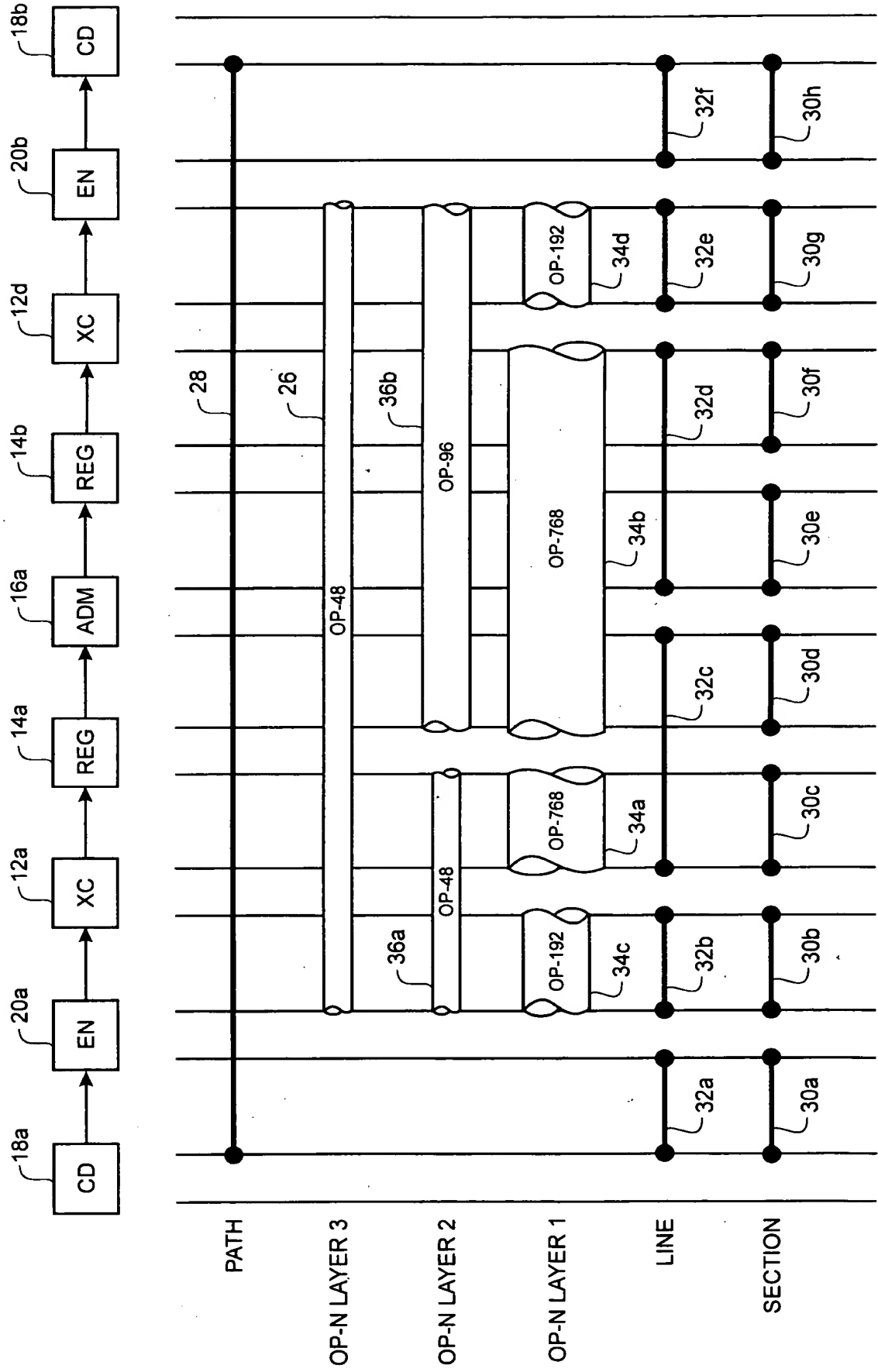
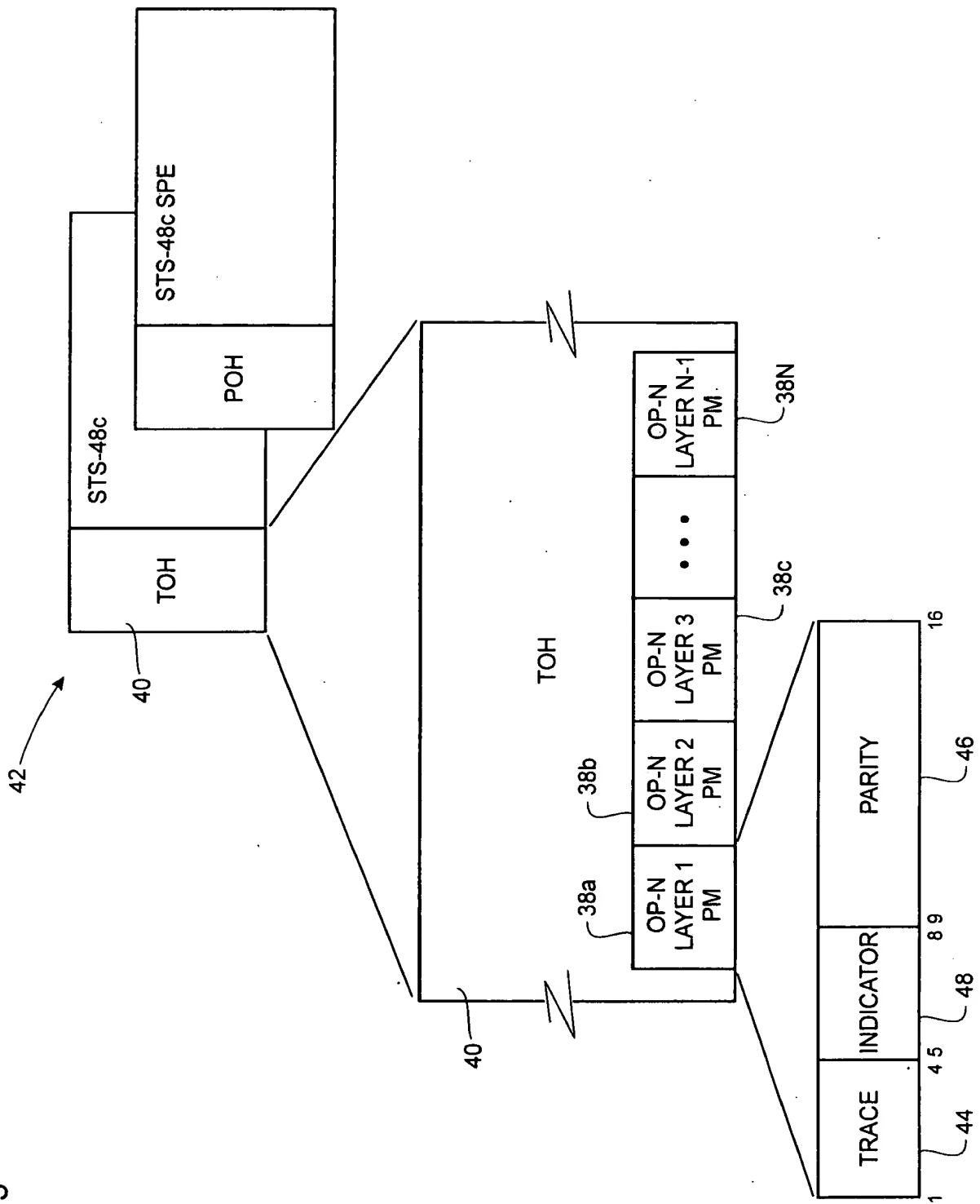


Figure 3



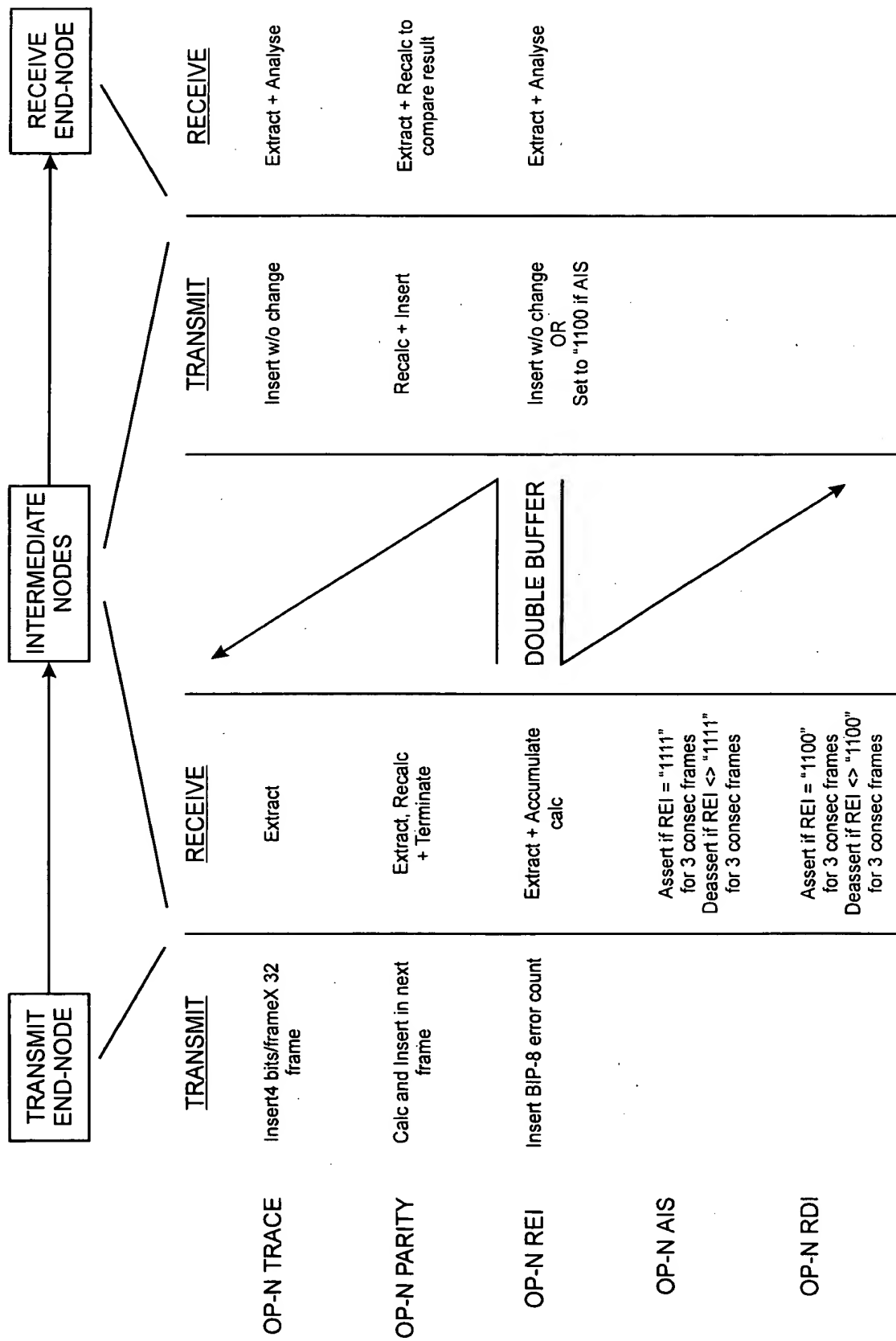
[illegible]

FIG. 5 is a block diagram of a system 50 for data transmission and reception. The system 50 includes a memory 64, a parity comparator 66, a fault indication processor 62, a double buffer 56, a combiner 58, an elastic store 54, and a pointer processor state machine 60. The system 50 is configured to receive data and transmit data.

Figure 5

